SPECIFICATION
[Electronic Version 1.2.8]

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CIRCUIT SIMULATOR SYSTEM AND METHOD

Background of the Invention

[p1]This invention relates to methods and systems used for generating behavioral models used in integrated circuit design. More particularly, the present invention provides for a new behavioral model that provides timing, noise and integrity grid analysis.

[p2] When simulating I/O electrical performance during timing characterization, signal integrity analysis, and power grid integrity analysis, various I/O modeling techniques have been used. At one end of the modeling spectrum are the full netlist models that contain detailed architectural and parasitic information of the I/O. These models provide the highest level of accuracy and can be used for a variety of analysis. A major disadvantage of full netlist models are excessive simulation times that prohibit them from being used at the chip level and non convergence under certain conditions. At the other end of the spectrum are empirical models for driver delay and IBIS models for signal integrity analysis.

[p3] Empirical models use simple equations or lookup tables for predicting driver delay and output slew rate. The advantage of empirical models is fast simulation time. The disadvantages are poor accuracy under certain conditions, and they are typically limited to timing analysis. For signal integrity analysis IBIS models can be used. The advantage of these models are accurate driver output waveforms across a wide range of loading conditions. The disadvantages are they cannot be used for

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The original specification has been replaced JP 1/30/06

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Stylesheet Version 1.0

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[0002] When simulating I/O electrical performance during timing characterization, signal integrity analysis, and power grid integrity analysis, various I/O modeling techniques have been used. At one end of the modeling spectrum are the full netlist models that contain detailed architectural and parasitic information of the I/O. These models provide the highest level of accuracy and can be used for a variety of analysis. A major disadvantage of full netlist models are excessive simulation times that prohibit them from being used at the chip level and non-convergence under certain conditions. At the other end of the spectrum are empirical models for driver delay and IBIS models for signal integrity analysis.

[0003] Empirical models use simple equations or lookup tables for predicting driver delay and output slew rate. The advantage of empirical models is fast simulation time. The disadvantages are poor accuracy under certain conditions, and they are typically limited to timing analysis. For signal integrity analysis IBIS models can be used. The advantage of these models are accurate driver output waveforms across a wide range of loading conditions. The disadvantages are they cannot be used for timing analysis and the models do not predict driver sensitivity to variations in supply voltage, temperature, and input slew rate.

[0004] I/O behavioral modeling in the form of IBIS models has gained wide acceptance in